

REMARKS

The specification and Fig. 4 have been amended to correct inadvertent errors. The support for the amendments is shown in original claim 2 and the description on page 16, lines 18-26 of the specification relating to the operation of the subtracter 339. No new matter has been added.

Claims 19-20 stand rejected under 35 U.S.C. § 112, first paragraph. Independent claim 19 has been amended to address this rejection, withdrawal of which is respectfully requested.

Claims 19-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Shih et al. Claim 19 has been amended to describe the features of the present invention for calculating a phase error of the clock signal based on the difference between first and second sample values, and the difference between second and third sample values of consecutive first, second and third sample values of the readout signal. These features are indicated in the Office Action to be allowable with respect to claim 1. Accordingly, claims 19 and 20 are now also believed to be allowable.

Claims 19-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hamada et al. Applicants respectfully traverse this rejection for the reasons given above traversing the rejection under §102(b).

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

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FIG. 4

2 3 3

